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Thermal Analysis of Microelectronic Packages

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ABSTRACT

The temperature field produced in microelectronic packages can be extremely complex due to the conjugate interaction between the cooling fluid and the numerous components of the package and board, which generally consist of a wide range of materials with differing properties. Although a variety of numerical solution techniques are available for solving the basic heat transfer equations within the fluid and solid domains, the regular geometry of microelectronics components allows for successful implementation of efficient analytic-integral type methods. This study uses a Fourier series minimization procedure to solve for the three-dimensional steady-state temperature field within a package containing heat generating die. The establishment of package thermal resistances then allows for simple coupling with a PCB model for solution of fluid-side film coefficients and board temperatures.

A variety of package types are considered, including plastic encapsulants, cavity up and cavity down ceramic designs, and the effects of module geometry and thermophysical properties are examined for both single-chip (SCP) and multichip (MCP) packages. Convective boundary conditions are imposed on all exposed surfaces, including approximations with regards to leadframe modelling, heat sinks and die attachment.

Examples are given showing typical operating temperature levels and thermal resistances of ceramic and plastic-type packages, both for SCP and MCP assemblies. A standard thermal resistance optimization criterion is proposed which considers the relevance of heat-sink cooling, package construction strategy, and on-board placement of these packages. This provides a convenient measure of the conceived package design as an efficient choice for heat transfer. Experimental data is reported to substantiate the accuracy of the model.

Nomenclature

 $a_{m,n},b_{m,n}$

Bi	Biot Number, $\equiv (h \cdot L)/k$
$f_{m,n}, g_{m,n}$	interlayer functions
h	heat transfer coefficient, $W/(m^2 \cdot K)$
$I^{(1)}, I^{(2)}$	integrals in least squares analysis
J_s	total number of integration sections
k	thermal conductivity, $W/(m \cdot K)$
L_1, L_2	package length in x and y direction, respectively, m
M	total number of layers in cap plus M_2
M_1	total number of layers in base cell
M_2	total number of layers in side wall plus
795. * 0	M_1
N	series truncation limit
P_H	package to board height (spacing) (m)
	heat flux density, W/m^2
R	thermal resistance °C/W
$egin{array}{l} q \ R \ S_1,S_2 \end{array}$	bottom and top surface of the cell, respectively
t _i	layer thickness, m
\dot{T}	temperature, °C
w_1w_4	ceramic side wall dimensions, m
W_1,W_4	package-board placement positions, mm
$X_i(x), Y_i(y), Z_i(z)$ Coordinates	separation variables
x, y, z	cartesian coordinates
Greek Symbols	
α	auxiliary function
θ	temperature excess $\equiv T_i - T_{s,i}$, °C
Θ	temperature excess as given in Eq. 14, °C
€die, €cap, €bot	thermal radiation emissivities for cavity
The second second was only to be the let	die plane, cap plane, and bottom
	of package
$\epsilon_{m,i}$	separation constant
$\gamma_{m,n}$	effective separation constant
K	conductivity ratio between layers $\equiv k_i/k_{i+1}$
	$\equiv \kappa_i/\kappa_{i+1}$

Fourier series coefficients

separation constant $\lambda_{n,i}$ XY separation variable as given in Eq. 20 φ general eigenfunction coefficients $\Psi_{1,m,n},\Psi_{2,m,n}$ general eigenfunction coefficients $\Phi_{1,m,n}, \Phi_{2,m,n}$ Stefan-Boltzmann constant $\equiv 5.67 \times 10^{-8}, (W/m^2 \cdot K^4)$ Subscripts and Superscripts refers to a particular layer refers to an integration section series indices on coefficients m,n,p,qradiation temperature calculations; +273°C

1 Introduction

Heat transfer analysis of microelectronic devices has received considerable attention largely owing to the high flux levels associated with increased circuit densities. Excellent reviews concerning heat conduction and thermal design of microelectronic chips may be found in Ellison (1984), Bar-Cohen and Kraus (1990), Hartnett and Irvine (1990), and Aung (1991). Package taxonomy, as outlined by Aung (1991), can be considered in terms of four categories: (1) package interconnections - single chip package (SCP) and multichip package (MCP); (2) construction type - plastic and ceramic; (3) form factor - dual-in-line, quad, pin grid array lead-frames; (4) board attachment - through-hole, surface mount. An adequate and complete modeling of microelectronic packages must therefore address these basic categories owing to the wide variety of designs in the industry.

A large variety of numerical methods may be employed to model typical ceramic and plastic packages as shown in Figures 1 and 2. Computer-based analyses on these components can be split into two parts, basically (a) packages mounted on a board substrate with conjugate flow, and (b) individual packages with prescribed boundary conditions. In one case, the fluid-packageboard interaction is studied simultaneously, and in the other, the package and fluid-board are coupled but studied separately. Type (a) analyses are computationally cumbersome if posed simultaneously, since the governing differential equations are solved numerically for both the cooling air stream and the package heat conduction (Yokono and Ishizuka, 1989). They are necessary however when dealing with complex flow situations in establishing/verifying local film coefficients. Type (b) analyses serve to address package performance, and may be combined with a fluidboard conjugate solution (Culham et al. 1991) in determining actual die plane temperature rise within a package under a given cooling situation. The basis of this study will be concerned with a type (b) procedure.

Finite-element modelling of typical packages has been treated by Ghorieshi and Nejib (1988), Rajala and Renksizbulut (1988), Furkay (1989). Owing to the regular, generally orthogonal geometry of microelectronic devices (i.e. rectangular), analytic-integral type methods have also been successfully developed and used. Idealized chip conditions were modeled in this way by Gray et al. (1974) using Green's functions. Haji-Sheikh and Beck, in Aung (1991, Ch. 6), outline a Green's function solution procedure which results in a standard set of integral equations to be solved for multiple layered materials with mixed boundary conditions. Estes (1989) used an attractive combined Fourier transform / adjoint solution technique in modelling chip-on-board (COB) systems. Lemczyk, Culham and Yovanovich (1989) outlined a Fourier-separable solution procedure applied to multilayered PCB substrates with forced convection, mixed boundary conditions. An analytical Fourier model, having idealized uniform boundary conditions, was also presented by Lee, Palisoc and Min (1989). Their model is but a subset of a more generalized solution, allowing for multiple layers and mixed boundary conditions, which will be presented in this study.

This work will cover the following areas. First, a steady-state, three-dimensional heat conduction model for microelectronic packages is outlined which allows for adequate variation of parameters in each of the four design categories outlined above. The solution methodology is similar to the one used in Lemczyk, Culham and Yovanovich (1989) but applied to particular package constructions. Secondly, a standard package optimization reference is presented. This describes the most ideal package cooling situation, i.e. where all exposed package surfaces are prescribed by the ambient coolant temperature. From this, a measure of performance from the convection, radiation and leadframe resistances can be compared. Finally, numerical and experimental results are presented for typical ceramic and plastic package assemblies.

2 Theory

2.1 Preliminary Base Cell Analysis

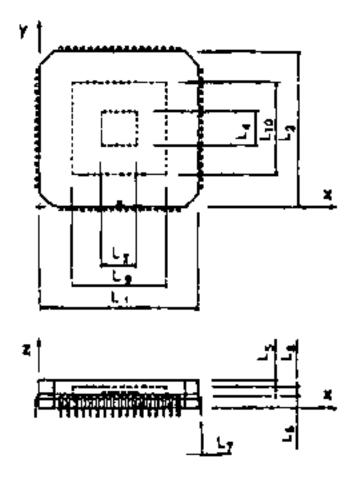
The three-dimensional heat conduction solution for generic ceramic and plastic packages shown in Figs. 1 and 2, will rely on a fundamental solution obtained for a typical rectangular multi-layered base cell shown in Fig. 3. Each homogeneous layer, with thermal conductivity k_i , has a general convective boundary condition at the four side faces.

The origin of the individual layer coordinate systems x_i, y_i, z_i is located at the lower left corner as illustrated in Fig. 3 for layer 1. A separable solution can be formed in a straightforward manner, where the temperature field in each layer, T_i , is given as

$$\theta_i(x,y,z) = \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} X_i(x) Y_i(y) Z_i(z) ; \quad \theta_i = T_i - T_{s,i} \quad (1)$$

where

$$X_{i}(x) = \cos(\epsilon_{m,i}x/L_{1}) + \frac{Bi_{1,i}}{\epsilon_{m,i}}\sin(\epsilon_{m,i}x/L_{1}) \qquad (2)$$



- L₁ Pockage width in x-direction L₂ Package width in y-direction
- Ls Die width in x-direction
 L. Die width in y-direction
- Le Substrate thicknessess
 Ly Lead frame thickness

Lg Cap Ihicknoss

- La Sidewall thicknesses
 La Internal cavity x—width
 Lio Internat covity y—width
- ks Cop conductivity
- ks Substrate conductivities
- ky Lead frame canductivity
- kg Sidewall conductivities
- E₁ case emissivity
 E₂ cavity emissivity

Figure 1: Typical Ceramic Package

$$Y_i(y) = \cos(\lambda_{n,i}y/L_2) + \frac{Bi_{3,i}}{\lambda_{n,i}}\sin(\lambda_{n,i}y/L_2)$$
 (3)

$$Z_i(z) = a_{m,n}^{(i)} \cosh(\gamma_{m,n}^{(i)} z/L_1) + b_{m,n}^{(i)} \sinh(\gamma_{m,n}^{(i)} z/L_1) \quad (4)$$

$$\epsilon_{m,i}: \qquad \left(\epsilon_{m,i}^2 - Bi_{1,i}Bi_{2,i}\right)\sin(\epsilon_{m,i}) - \\ \epsilon_{m,i}\left(Bi_{1,i} + Bi_{2,i}\right)\cos(\epsilon_{m,i}) = 0$$
 (5)

$$\lambda_{n,i} : \left(\lambda_{n,i}^2 - Bi_{3,i}Bi_{4,i} \right) \sin(\lambda_{n,i}) -$$

$$\lambda_{n,i} \left(Bi_{3,i} + Bi_{4,i} \right) \cos(\lambda_{n,i}) = 0$$
(6)

$$Bi_{1,i} = \frac{h_{1,i}L_1}{k_i}$$
; $Bi_{2,i} = \frac{h_{2,i}L_1}{k_i}Bi_{3,i} = \frac{h_{3,i}L_2}{k_i}Bi_{4,i} = \frac{h_{4,i}L_2}{k_i}$ (7)

$$\gamma_{m,n}^{(i)} = \sqrt{\epsilon_{m,i}^2 + \left(\frac{L_1}{L_2}\lambda_{n,i}\right)^2}$$
 (8)

$$\Delta\theta_i = T_{s,i} - T_{s,i+1} \; ; \quad \kappa_i = \frac{k_i}{k_{i+1}} \tag{9}$$

The forms above assume that a single $T_{s,i}$ is specified for each layer at it's side faces; $h_{1,i}$ to $h_{4,i}$, may have different values. The double series in (1) will each be truncated by a single N value.

Adjacent layers are in perfect contact with each other, thus satisfying the following boundary conditions along the whole of each interface,

$$\theta_i(x,y,t_i) = \theta_{i+1}(x,y,0) , \qquad (10)$$

$$\kappa_i \frac{\partial \theta_i}{\partial z}(x, y, t_i) = \frac{\partial \theta_{i+1}}{\partial z}(x, y, 0) ; \kappa_i = \frac{k_i}{k_{i+1}}. \tag{11}$$

On the top plane surface, S_2 , in Fig. 3 ($z = t_{M_1}$ of layer M_1) a general convective boundary condition will be imposed of the

$$L_1 \frac{\partial \theta_{M_1}}{\partial z}(z, y, t_{M_1}) + Bi_{eff}^{(j)}(\theta_{M_1} - \Theta_{eff}^{(j)}) = \frac{q^{(j)}L_1}{k_{M_2}}$$
(12)

where

$$Bi_{eff}^{(j)} = \frac{h^{(j)}L_1}{k_{M_1}}$$
 (13)

$$\Theta_{eff}^{(j)} = T_{M_1}^{(j)} - T_{\bullet,M_1} \tag{14}$$

and j denotes a particular x, y rectangular integration section. Hence we can write (12) in the form

$$\sum_{m=1}^{\infty} \sum_{n=1}^{\infty} (\Psi_{1,m,n} a_{m,n}^{(M_1)} + \Psi_{2,m,n} b_{m,n}^{(M_1)}) = \frac{q^{(j)} L_1}{k_{M_1}} + Bi_{eff}^{(j)} \Theta_{eff}^{(j)}$$
 (15)

where

$$\Psi_{1,m,n} = (\gamma_{m,n}^{(M_1)} \sinh(\gamma_{m,n}^{(M_1)} t_{M_1}/L_1) + Bi_{eff}^{(j)}$$

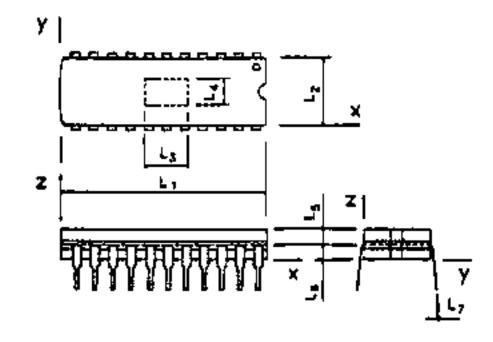
$$\cosh(\gamma_{m,n}^{(M_1)} t_{M_1}/L_1))\phi_{m,n}^{(M_1)}$$
(16)

$$= \Phi_{1,m,n} \phi_{m,n}^{(M_1)} \tag{17}$$

$$\Psi_{2,m,n} = (\gamma_{m,n}^{(M_1)} \cosh(\gamma_{m,n}^{(M_2)} t_{M_1} / L_1) + Bi_{eff}^{(j)}$$

$$\sinh(\gamma_{m,n}^{(M_1)} t_{M_1} / L_1)) \phi_{m,n}^{(M_1)}$$
(18)

$$= \Phi_{2,m,n} \phi_{m,n}^{(M_1)} \tag{19}$$



Package width in x-direction Package width in y-direction

ks Cap conductivity ks Substrate conductivities ky Lead frome conductivity

Die width in x-direction Die width in y-direction

Cap finickness to die level

E. case emissivity

Substrate thicknessess

L₇ Lead frome thickness

Figure 2: Typical Plastic Package

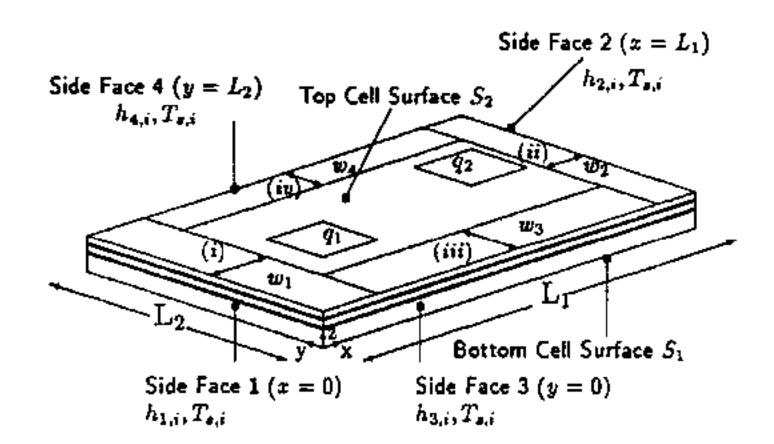


Figure 3: 3D Base Cell

and
$$\phi_{m,n}^{(M_1)} \equiv X_{M_1}(x)Y_{M_1}(y)$$
 (20)

By approximating the boundary conditions in a least-squares sense w.r.t. the coefficients $a_{m,n}^{(M_1)}$, and using N terms in each series, we can obtain the set of equations

$$[\Psi_{1,p,q}\Psi_{1,m,n}]a_{m,n}^{(M_1)} + [\Psi_{1,p,q}\Psi_{2,m,n}]b_{m,n}^{(M_1)} = \{\Psi_{1,p,q}r^{(j)}\}$$
 (21)

$$[\Psi_{1,p,q}\Psi_{1,m,n}] = \sum_{i=1}^{J_t} \Phi_{1,p,q}\Phi_{1,m,n} \int \int_j \phi_{m,n}^{(M_1)} \phi_{p,q}^{(M_1)}$$
(22)

$$[\Psi_{1,p,q}\Psi_{2,m,n}] = \sum_{i=1}^{J_t} \Phi_{1,p,q} \Phi_{2,m,n} \int \int_j \phi_{m,n}^{(M_1)} \phi_{p,q}^{(M_1)}$$
 (23)

$$\{\Psi_{1,p,q}\tau^{(j)}\} = \sum_{i=1}^{J_s} \Phi_{1,p,q} \left(\frac{q^{(j)}L_1}{k_{M_1}} + Bi_{eff}^{(j)} \Theta_{eff}^{(j)} \right) \int \int_J \phi_{p,q}^{(M_1)} \quad (24)$$

In the above, J_s is the total number of rectangular integration sections covering the entire S_2 plane. A general sectional convective boundary condition (i.e. mixed) such as (12) could also be assumed for the bottom plane surface (z=0) of layer 1, as shown by Lemczyk et al.(1989). However, by assuming uniform convection over the bottom $(0 \le x \le L_1, 0 \le y \le L_2)$ surface then

$$b_{m,n}^{(1)} = f_{m,n}^{(1)} + g_{m,n}^{(1)} a_{m,n}^{(1)}$$
 (25)

$$f_{m,n}^{(1)} = \frac{-2(Bi_{bot}\Theta_{bot} + q_{bot})\sin(\epsilon_{m,1})\sin(\lambda_{n,1})}{\gamma_{m,n}^{(1)}(\lambda_{n,1} + \sin(2\lambda_{n,1})/2)(\epsilon_{m,1} + \sin(2\epsilon_{m,1})/2)} (26)$$

$$g_{m,n}^{(1)} = \frac{Bi_{bot}}{\gamma_{m,n}^{(1)}} \tag{27}$$

A recursive algorithm using the interlayer relations (10) and (11), is given as follows. Initialization values:

$$g'_{1,m,n,p,q} = 1$$
 $g'_{2,m,n,m,n} = g^{(1)}_{m,n}$
 $g'_{3,m,n} = 0$ $g'_{4,m,n} = f^{(1)}_{m,n}$ (28)

Auxiliary functions:

$$\alpha_1 = \cosh(\gamma_{m,n}^{(i)} t_i / L_1) I_{m,n,p,q}^{(1)}$$
 (29)

$$\alpha_2 = \sinh(\gamma_{m,n}^{(i)} t_i / L_1) I_{m,n,n,n}^{(1)} \tag{30}$$

$$\alpha_3 = \Delta\Theta_i I_{m,n}^{(2)} \tag{31}$$

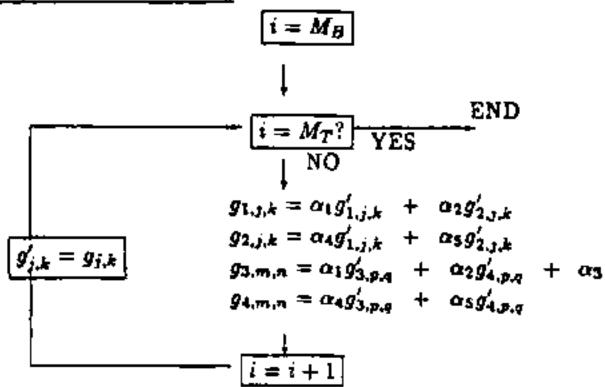
$$\alpha_4 = \kappa_i \gamma_{m,n}^{(i)} \alpha_2 / \gamma_{m,n}^{(i+1)}$$
 (32)

$$\alpha_5 = \kappa_i \gamma_{m,n}^{(i)} \alpha_1 / \gamma_{m,n}^{(i+1)} \tag{33}$$

$$I_{m,n,p,q}^{(1)} = \frac{\int_0^{L_1} X_{p,i} X_{m,i+1} dx \int_0^{L_2} Y_{q,i} Y_{n,i+1} dy}{\int_0^{L_1} X_{m,i+1}^2 dx \int_0^{L_2} Y_{q,i+1}^2 dy} \qquad (34)$$

$$I_{m,n}^{(2)} = \frac{\int_0^{L_1} X_{m,i+1} dx \int_0^{L_4} Y_{n,i+1} dy}{\int_0^{L_1} X_{m,i+1}^2 dx \int_0^{L_6} Y_{n,i+1}^2 dy}$$
(35)

If $M_T - M_B > 0$, then do:



else: use initialized values for the g functions in (28).

In the above algorithm, the j,k indices are defined by $j \equiv (m-1)N + p$ and $k \equiv (n-1)N + q$. Also M_T and M_B denote the topmost and bottommost layer indices.

Using the above algorithm, we can then write the $a_{m,n}^{(M_1)}$, $b_{m,n}^{(M_2)}$ in terms of the $a_{m,n}^{(1)}$. Substituting into (19), we can obtain a final set of equations for the base cell in Fig. 3,

$$\begin{aligned}
&\{[\Psi_{1,p,q}\Psi_{1,m,n}][g_1] + [\Psi_{1,p,q}\Psi_{2,m,n}][g_2]\} a_{m,n}^{(1)} \\
&= \{\Psi_{1,p,q}r^{(i)}\} - [\Psi_{1,p,q}\Psi_{1,m,n}]\{g_3\} \sim \{\Psi_{1,p,q}\Psi_{2,m,n}\}\{g_4\}
\end{aligned}$$
(36)

to solve for the unknown $a_{m,n}^{(1)}$. The solution procedure described above therefore determines the three-dimensional temperature field within a multi-layered base ceil. The plastic packages are modelled having two (2) such cells (referred to as a die and cap ceil) joined along their common S_2 planes. The ceramic packages have the die and cap cells joined by side walls (i.e. at regions (i) to (iv)) thus forming the interior cavity (hermetic) zone of the ceramic package.

2.2 Plastic Package Analysis

For the plastic package shown by Fig. 4, the interfacial boundary conditions between the die cell plane and cap cell become,

$$\theta_{M_2} = \theta_{M_1} + \Delta \theta_{M_1}, \ 0 \le x \le L_1, \tag{37}$$

$$\frac{\partial \theta_{M_1}}{\partial z} = \kappa_{M_1}^{-1} \frac{\partial \theta_{M_2}}{\partial z} + \frac{q^{(j)}}{k_{M_1}}, \ 0 \le z \le L_1 \tag{38}$$

These satisfy both temperature and heat flux continuity for the die and cap cell attachment.

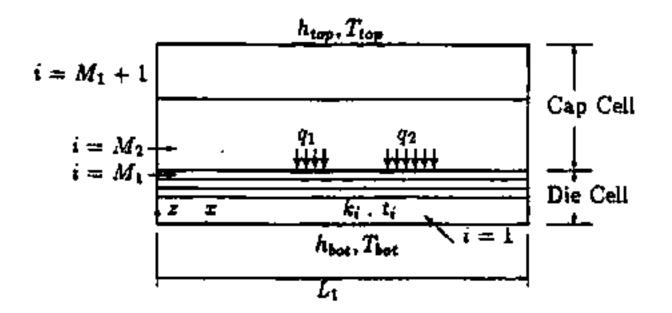


Figure 4: Plastic Package Analysis; 2D Cross-Section

A set of equations similar to (36) above can be obtained which relate $a_{m,n}^{(M_1)}, b_{m,n}^{(M_2)}, a_{m,n}^{(M_2)}, b_{m,n}^{(M_2)}$. The above recursive algorithm used on both die and cap cells eventually can reduce this set of equations to a single set of unknown coefficients $a_{m,n}^{(1)}$ in the final matrix equation (Lemczyk and Culham (1989)).

2.3 Ceramic Package Analysis

The base cell procedure described above is used to obtain solutions to typical multi-layered die and cap cells of a ceramic package as shown in Fig. 5. These cells are connected by side wall layers, attached at regions (i) to (iv) (at the die base cell S_2 plane, and at corresponding regions (v) to (viii) of the cap cell S_2 plane), which were modelled using simple one-dimensional fin equations

$$\theta_i = T_i - T_{\epsilon,i} = a_i \cosh(\epsilon_i z) + b_i \sinh(\epsilon_i z) \tag{39}$$

with

$$\epsilon_i^{(i)} = \sqrt{Bi_{1,i}/(L_1w_1)} ; \epsilon_i^{(ii)} = \sqrt{Bi_{2,i}/(L_1w_2)}$$
 (40)

$$\epsilon_i^{(iii)} = \sqrt{Bi_{3,i}/(L_2w_3)} \; ; \; \epsilon_i^{(iv)} = \sqrt{Bi_{4,i}/(L_2w_4)}$$
 (41)

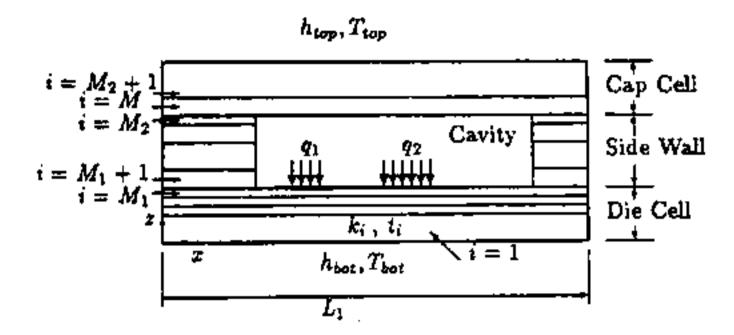


Figure 5: Ceramic Package Analysis; 2D Cross-Section

The die to cap cell attachment was modeled through effective conductances h_{eff} found by

$$h_{eff,(i)} = \frac{q_{M_2,(i)}}{T_{eff,(i)} - T_{eff,(v)}}; h_{eff,(ii)}$$

$$= \frac{q_{M_2,(ii)}}{T_{eff,(ii)} - T_{eff,(vi)}}$$

$$h_{eff,(iii)} = \frac{q_{M_2,(iii)}}{T_{eff,(iii)} - T_{eff,(viii)}}; h_{eff,(iv)}$$

$$= \frac{q_{M_2,(iv)}}{T_{eff,(iv)} - T_{eff,(viii)}}$$
(43)

where the q_{M_2} denote the total heat flow entering through the cap regions (v) to (viii).

A recursive algorithm for relating multiple side wall layer coefficients in (39) can be easily derived using (10) and (11); details may be found in Lemczyk and Culham (1989).

Cavity heat exchange between die and cap planes consists of radiation and convective components. The boundary conditions in the cavity zone for die and cap cells become

$$L_1 \frac{\partial \theta_M}{\partial z} - B i_{cap} (\theta_M - \theta^{(dis)}) = 0 (44)$$

$$L_1 \frac{\partial \theta_{M_1}}{\partial z} + Bi_{die}(\theta_{M_1} - \theta^{(cap)}) = \frac{q_j L_1}{k_{M_1}}$$
 (45)

where

$$\theta^{(die)} = T^{(die)} - T_{s,M} ; Bi_{cep} = \frac{h_{cep}L_1}{\bar{k}_{M}}$$
 (46)

$$\theta^{(cap)} = T^{(cap)} - T_{s,M_1} ; Bi_{dic} = \frac{h_{dic}L_1}{k_{M_1}}$$
 (47)

The effective coefficient h_{cap} is comprised of both radiation and convection coefficients, assuming a parallel resistance circuit, i.e.

$$h_{cap} = h_R^{(cap)} + h_{conv} (48)$$

$$h_{die} = h_{R}^{(die)} + h_{conv} (49)$$

The effective radiation coefficients become

$$h_R^{(die)} = \frac{\epsilon_{die}\sigma((T_R^{(die)})^4 - (T_R^{(cap)})^4)}{T_R^{(die)} - T_R^{(cap)}}$$
(50)

$$h_R^{(tap)} = \frac{\epsilon_{cap}}{\epsilon_{die}} h_R^{(die)}$$
 (51)

For pure conduction through the air in the cavity, h_{conv} is simply given as

$$h_{conv} = k_{AIR}/t_{cavity} (52)$$

The mean cavity plane temperatures T_R required for cavity radiation exchange, and the side wall coefficients $h_{eff,(i)}$ to $h_{eff,(iv)}$ necessitate an iterative solution between cap and die base cells.

2.4 Peripheral Analyses

Die Attachment

The heat flux specification in (12), (38) and (45) can be easily adjusted to include an individual die attachment thermal resistance, R_{die} , which accounts for a die epoxy resistance with or without a thermal vias network resistance (Lee *et al.* 1991). The form (45) for instance becomes modified by a factor

$$f_{die} = \frac{1}{(1 + h_{die} A_{die} R_{die})} \tag{53}$$

such that

$$L_1 \frac{\partial \theta_{M_1}}{\partial z} + Bi_{dic} f_{dic} \left(\theta_{M_1} - \theta^{(cop)} \right) = \frac{q_j L_1}{k_{M_1}} f_{dic}$$
 (54)

where A_{die} is the individual die area. The resulting solution for θ_{M_1} will therefore give temperatures at the die plane level (i.e. at $z=t_{M_1}$ of layer M_1). However, where $q_j\neq 0$, an actual mean chip plane temperature $\overline{\theta_c}$ can be evaluated by

$$\overline{\theta_c} = \overline{\theta_D} + Q_{dis} R_{dis}, \tag{55}$$

where θ_D is the mean temperature rise at the die plane level, and Q_{die} is the net heat flow rate into the die plane.

Heat Sinks

By referring to Figs. 4 and 5, it is easily seen that the package top coefficient h_{top} can be treated as an effective conductance coefficient for a particular heat sink fin model. A variety of heat sink types, including omni-directional stacked fins (Wesling, 1988), longitudinal (ribbed style), and pin-type fins, have been studied (Bar-Cohen and Kraus, 1990). An effective conductance for these can be obtained easily, as noted in Lemczyk and Culham (1990), for use as an h_{top} value.

Leadframe Modeling

The packages shown in Figs. 1 and 2 illustrate two types of package leadframe types, namely quad (4 sided) and dual in-line (2 sided). A third type, pin-grid array, can also be modeled but is not considered in this work.

The leadframe is simulated by the uniform layer M_1 in both plastic and ceramic (cavity-up) packages shown in Figs. 4 and 5. The ceramic package may also have layer $M_1 + 1$ instead as the leadframe. The side film coefficients $h_{1,i}$ to $h_{4,i}$ are appropriately defined as follows.

Dual in-line : set h_{1,M_1} , $h_{2,M_1} = h_{LF}$

Quad: set h_{1,M_1} to $h_{4,M_1} = h_{LF}$

For the dual in-line, h_{3,M_1} and h_{4,M_1} are then set to film coefficient values as defined for other layers. In both cases, T_{4,M_1} is set to a local fluid sink temperature as for other layers. The effective leadframe coefficient h_{LF} can be determined through an individual fin analysis on a typical lead attached to a reference board temperature (Lemczyk and Culham, 1990). It is important to note that h_{LF} represents a mean conductance value; individual lead size, location and density of leads must be considered in establishing its value.

Cavity - Up/Down

The vertical orientation of the ceramic package shown in Fig. 5 illustrates a cavity-up model, with the heat source (die) locations found on layer M_1 . A cavity-down situation occurs where these heat sources are applied to surface S_2 of layer M, so that the lower cavity layer M_1 now receives heat via convection/radiation in the cavity. Equations (44) and (45) are easily manipulated to account for either cavity-up or cavity-down ceramic modeling. It is conceivable even that both layer surfaces M_1 and M could have applied heat sources simultaneously, in which case (44) and (45) would both have individual q_i specified.

Board Attachment

Both a surface-mount or gap-mount (through-hole) package-to-board attachment configurations can be adequately modelled using the above analyses. For a surface-mount package, h_{bot} becomes an effective epoxy conductance, and T_{bot} is a mean board reference temperature. These would be incorporated into Bi_{bot} , θ_{bot} in (26) and (27) with $q_{bot}=0$.

For a gap-mount situation, h_{bot} may be modeled as an effective radiation coefficient for exchange with the board T_{bot} surface, where

$$h_{bot} = \frac{\epsilon_{bot}\sigma(T_1^4 - T_{bot}^4)}{T_1 - T_{bot}} \tag{56}$$

Convection and conduction losses to a fluid (air) stream in the gap are modelled by setting

$$q_{bot} = \frac{2k_{AIR}L_1(T_1 - T_f)}{P_H k_1} \tag{57}$$

where T_1 represents a mean temperature of the bottom of package surface (z = 0 of layer 1). This necessitates iteration in the solution for a gap-mount package for establishing this temperature.

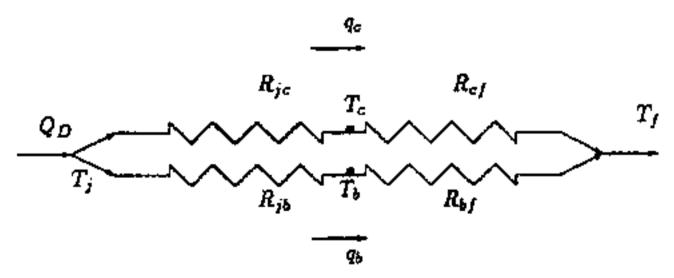


Figure 6: SCP Thermal Resistance Network

3 Thermal Resistance Characterization

Three distinct package thermal resistances are of paramount importance to the ensuing studies. These are defined as

$$R_{ja} = \frac{\overline{T_i} - T_f}{Q_i}$$
 (58)

$$R_{jb} = \frac{\overline{T_j} - T_{bat}}{Q_{jb}} \tag{59}$$

$$R_{jc} = \frac{\overline{T_j} - T_c}{Q_{jc}} \tag{60}$$

 R_{ja} is commonly defined as the junction-to-ambient thermal resistance for the package. In its above form, it represents an overall resistance between the mean junction temperature T_j and the ambient fluid sink temperature T_j , with Q_j being the total applied power to the particular die junction. It is important to note that this resistance inherently includes any film resistances on the package surfaces. R_{jb} and R_{jc} are respectively the junction-to-board and junction-to-case thermal resistances. All the above resistances may apply readily to MCP systems, in which case $\overline{T_j}$ must be computed as an overall multi-die average temperature. Q_j would then also be the sum of the individual die power levels.

Now it is important to note the proper interpretation and limitations of these thermal resistances. First, considering R_{14} , we note that the package analyses described previously required a T_{bot} board temperature value. As a result, any package solution, hence R_{ja} , relies directly on this specified board temperature. Unfortunately, T_{bot} can really only be determined from a PCB modeller in an iterative fashion, as noted in Culham et al. (1991). This fine but important point was also noted recently by Andrews (1988), Bar-Cohen et al. (1989), and Aung (1991, Ch.7), who concur with the configuration-specific nature of R_{ia} . This has often been overlooked or neglected in favour of a standard, vendorsupplied, R_{ja} for a particular package. The complete thermal circuit for any package containing one or more heat generating die, is shown in Figs. 6 and 7. R_{ef} is a case-to-ambient, and R_{bf} is the board-to-ambient thermal resistance. The resistances R_{cf} and R_{bf} are direct components of the heat flow path, and must be inherent in any procedure for estimating junction temperature rise. This can be seen through an equivalent form of equation (58) for a SCP,

$$R_{ja} = \frac{\overline{T_j} - T_f}{Q_j} = \left(\frac{1}{R_{ja} + R_{ef}} + \frac{1}{R_{jb} + R_{bf}}\right)^{-1}$$
 (61)

 R_{jb} and R_{jc} as shown, allow for convenient coupling to a PCB modeller in order to determine adequate local film coefficients for the package, and board temperatures. Q_{jb} is the total heat flow rate to the board T_{bot} reference, calculated from leadframe

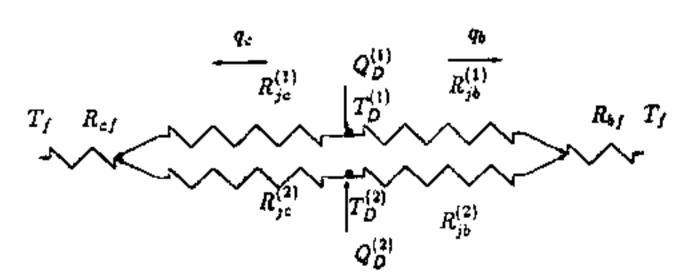


Figure 7: MCP Thermal Resistance Network

locations and from the package lower surface. Then, $Q_{jc} \equiv Q_j - Q_{jb}$, representing the total heat loss to the package case surfaces which are cooled by ambient temperatures.

4 Package Optimization

In studying the package models shown in Figs. 4 and 5, a variety of cooling enhancements could be proposed. However, the optimum cooling performance for these packages would be achieved if all the outer exposed surfaces had their film coefficients $\rightarrow \infty$, so that the outer package surface would be maintained at an ambient temperature T_f . For intrinsic purposes, we would set

$$T_{A,i} = T_{bot} = T_{top} = T_f \tag{62}$$

$$h_{s,i} = h_{bot} = h_{top} \quad \to \quad \infty \tag{63}$$

This isothermal-case package can then be considered as the optimal cooling configuration available (Lemczyk et al. 1991). Strategies such as heat-sink attachment, increased forced flow cooling conditions, or increased board thermal conductivity, merely enhance the boundary conditions on the package structure, towards this optimal limit.

We thus define

$$R_{opt} = \frac{\Delta T_O}{Q_i} \tag{64}$$

where ΔT_O is defined as the mean temperature difference between the die (junction) T_j and isothermal case reference temperature. It is important, however, to use the specific ambient temperature T_f as the isothermal case reference temperature, when comparing an actual package to this R_{opt} . We can additionally define a percentage optimization factor as

$$\mathcal{F}_{opt} = 100 \frac{R_{opt}}{R_{is}} \tag{65}$$

where R_{ja} is defined earlier. With respect to any cooling situation, having any combination of heat sink attachment, flow cooling, and board attachment, a particular package can be thus assessed on performance. It is important to note that the package construction, i.e. materials, geometry, die location, is inherently characteristic of the particular package. The above optimization factor reflects the boundary conditions, and not the structural design. Other factors on design optimization could also be introduced but are beyond the scope of this study. Andrews (1988), similarly realizing the dependence of package thermal performance on actual operating environment, introduced a figure of merit coefficient for performance description. In that work, a R_{jaO} was introduced, and was defined as the junction-to-ambient thermal resistance when board temperature was set to ambient temperature. It is important to note that this is not the same as the value of R_{apt} defined above, but is a subset of R_{ja} defined earlier.

A value of R_{opt} cannot be adequately obtained from experiment, and thus an accurate, theoretical-numerical estimate would be needed. As indirectly suggested by Bar-Cohen et al. (1989), vendor-supplied values of R_{opt} , accurately obtained numerically, would perhaps best serve the needs of package design and optimization, as proposed in the context of this study. Presently, R_{ja} values are supplied as standard resistances in industry, quoted under natural or forced convection conditions. The above analysis clearly shows the inadequacy of this approach, since these R_{ja} values are particularly dependent on the package-system placement and cooling conditions. In particular, as an example, the natural convection cooling of an isolated test package inside a closed box will not be the same as a package on board cooled in a channel flow situation, with other packages mounted on the board.

5 Package Simulations

Experimental results were obtained for typical plastic and ceramic packages, of SCP-type only, which were mounted on one side of a vertical, test coupon (FR-4 board) placed in a forced convection air stream (Mack, 1991). The package-coupon assembly was mounted in a small horizontal wind tunnel (20 cm × 20 cm working cross-section), with air drawn by two muffin-type fans and/or blower to obtain the desired free stream velocity. A 3.0 mm diameter pitot probe and micromanometer were used to measure velocity in the wind tunnel. Junction temperatures were measured using a Delco thermal sensitive test die, which contain two diodes and two resistors in a bridge arrangement. Package underside case temperature was measured using a 0.254 mm diameter copper-constantan (T-type) thermocouple. Lead frame temperatures were measured using 0.079 mm diameter chromel-alumel (K-type) thermocouples. Top surface temperatures of the package were measured with a UTi-9000 infrared camera. Low absorption, URTRANTM glass was located in the side of the wind tunnel test section to allow the temperature measurements by infrared camera. On-board placement of packages is shown in Fig. 8. The FR-4 board, with thermal conductivity $k_B = 0.4 \ W/mK$, was vertically oriented with respect to flow direction and gravity as shown. Dimensions and positioning details are given in Table 1. The following list describes the temperature measurements and locations.

 θ_t - maximum temperature rise on the top surface of the package (UTi camera), (°C)

 θ_{tavg} - average package top surface temperature rise (Uti), (°C)

 θ_j - junction temperature rise (Delco die), (°C)

 θ_b - temperature rise at the center of underside of package (T-type t.c.), (°C)

 θ_{ki} - lead temperature rises : PLCC, i= 1 to 4 or i=1 to 6 (K-type t.c.), located at side leads (see Fig. 9.) (°C)

Fig. 9 shows the particular θ_{ki} leadframe thermocouple locations for the packages studied.

Package and board specifications are given in Table 1. A plastic quad (PLCC-68 pin) package was tested and modelled, along

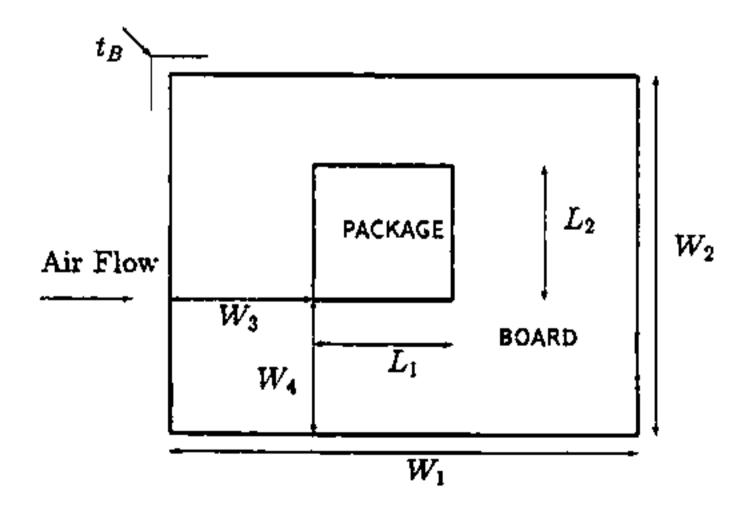


Figure 8: Package-Board Configuration

with four ceramic packages: a quad (CQUAD-84 pin), a dual in-line dip, with leads (major axis) oriented vertically or horizontally with respect to flow direction (CRDPV, CRDPH -24 pin), and a leadless ceramic chip carrier package (LLCCC-44 pin). The LLCCC was surface mounted, and all others were gap-mounted to the test coupon, with leads penetrating through the board thickness.

Experimental and numerical temperature predictions are shown in Table 2, along with thermal resistance values. Numerical results were obtained using, on average, N=10 terms as the Fourier series truncation limit. This was found to converge temperatures within $\pm 2\%$ and resistances within $\pm 5\%$. The board simulation to establish the local package fluid film coefficients was made using META (Culham et al. 1991). It is important to note that the h_{avg} film coefficient shown in Table 2 includes a radiation component. Radiation emissivities are noted in Table 1.

PLCC results in Table 2 show good agreement between the numerical and experimental data. The CQUAD junction temperatures exhibit close agreement, but as with the remaining ceramic packages shown, the case temperatures are not adequately simulated, i.e. the experimental data indicates higher case temperatures (approx 5 $^{\circ}C$). The numerical simulations show little difference in results for the ceramic packages for the two different velocity flow fields. The experimental results are similar, since thermocouple measurement error is $\pm 1^{\circ}C$, except for the LLCCC junction temperature measurements. Die attach thermal resistances were not used in the simulations, which could explain the slightly lower junction temperatures being predicted. Also shown in Table 2 are thermal resistances obtained numerically, including \mathcal{F}_{opt} , and vendor-supplied quoted R_{ja}^{ν} values. R_{ja}^{ν} for the LLCCC package could not be obtained at this point. The R_{ja}^{v} values shown were experimentally obtained under typical still air (natural convection) conditions, inside a one cubic foot volume plastic box. As can be seen, these are quite a bit higher than the predicted forced convection results. The inadequacy of using supplied R_{ja}^{ν} values can thus be appreciated, since an actual package may behave very differently than ideal testing. The \mathcal{F}_{opt} criterion however, at least provides a measure of performance by which a package and system may be further optimized.

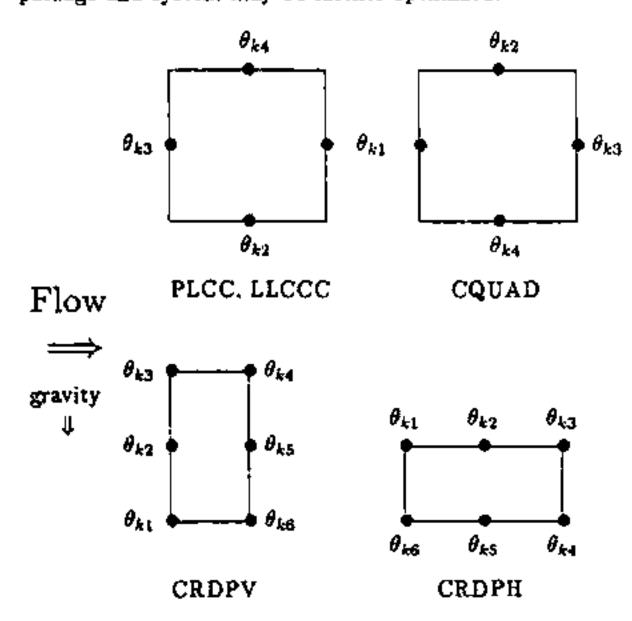


Figure 9: Lead Thermocouple Locations

		,	•	_						
(mm)	PLCC	CQUAD	CRDPV	CRDPH	rrccc					
BOARD SPECIFICATIONS										
W_1	110	51	75	75	51					
W_2	140	51	75	75	51					
W_3	40.4	11.7	31	20	17.1					
W_4	77.9	11.7	20	31	17.1					
t _B	1.6	1.6	1.8	1.8	1.8					
PACKAGE SPECIFICATIONS										
L_1	24.1	27.6	13.2	31.8	16.5					
L_2	24.1	27.6	31.8	13.2	16.5					
L_3	6.35	5.96	5.08	5.08	4.01					
L_4	6.35	5.96	5.08	5.08	4.01					
L_5	1.42	1.02	0.81	18.0	0.51					
L_6	2.54	0.80	1.32	1.32	0.64					
L_7	0.26	0.20	0.20	0.20	0.20					
La	† -	1.6	1.5	1.5	0.51					
L ₉	١-	15.24	6.4	6.6	9.9					
L_{10}	i -	15.24	6.6	6.4	9.9					
k ₅	0.63	16.7	16.7	16.7	16.7					
k ₆	0.63	16.7	16.7	16.7	16.7					
k ₇	300	11	11	11	11					
k _B	-	16.7	16.7	16.7	16.7					
Edia	0.9	0.5	0.5	0.5	0.5					
Ccap	•	0.9	0.9	0.9	0.9					
Ebal	0.9	0.9	0.9	0.9	0.9					

Table 1: Package-Board Specifications

6 Conclusions

An indepth, steady-state thermal analysis of microelectronic packages has been presented, using a versatile, analytical-numerical Fourier technique, which allows for adequate geometric, thermophysical and boundary condition modeling. Package thermal resistances were outlined, and a package optimization criterion was proposed. Numerical simulations were performed and compared to experimental results.

It is important to note the contributions of this work as compared to what is currently available in the literature. The study showed that accurate temperature prediction of microelectronic packages can be achieved without resort to extremely cumbersome, full-domain numerical procedures. Instead, an iterative solution between a package and board-side modeler, as presented, can be used quite adequately, with tremendous computational-time savings for the analysis. Even though the results shown were for a single package-on-board system, multiple packages on board can be modeled in a similar manner. The local package film coefficients and ambient temperature can be obtained from the board modeler, and input to the package modeler to obtain individual package temperatures, and thermal resistances.

An optimization factor for microelectronic packages was de-

	PLCC		CQUAD		CRDPV		CRDPH		LLCCC		
Power (W)	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	
$U_{\infty}(m/s)$	3.5	5.1	3.5	5.2	3.5	5.0	3.3	4.9	3.5	4.9	
T_{∞} (°C)	20.9	20.0	21.5	21.5	21.4	21.6	21.4	21.4	21.5	21.6	
Experimental Temperatures (°C)											
θ_t	9.0	8.9	4.6	3.5	7.3	6.2	7.9	6.7	11.0	9.9	
θ_{tavg}	5.2	5.4	4.1	2.9	6.5	5.5	6.9	5.9	9.6	8.6	
θ_j	12.2	11.3	11.8	10.9	10.2	8.3	10.7	9.2	15.6	11.3	
θ_b	7.5	6.7	4.4	3.5	6.5	5.2	6.2	5.4	11.9	10.4	
θ_{k1}	5.9	5.1	2.0	1.3	3.8	2.7	3.7	3.0	10.0	8.4	
θ_{k2}	4.9	4.2	2.7	1.9	4.4	3.2	5.6	4.7	10.8	9.3	
θ_{k3}	4.5	3.5	3.4	2.7	3.5	2.5	5.1	4.3	9.2	7.8	
θ _{k4}	4.1	3.5	2.7	1.9	4.8	3.5	4.7	3.9	9.0	8.5	
θ _{k5}	-	-		_	6.2	4.8	5.6	4.7	_	_	
θ_{k6}	-	_	-	_	4.6	3.3	3.2	2.6	-		
Numerical Temp	eratur	e Pred	ictions	(°C)							
$h_{avg}(W/m^2C)$	45.2	53.6	48.8	58.5	50.0	58.9	45.1	53.9	49.9	58.5	
θ_t	8.4	7.3	0.1	0,1	0.0	0.0	0.0	0.0	0.2	0.2	
θ_{tavg}	7.4	6.3	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	
θ_j	9.5	8.3	9.6	9.6	4.8	4.7	4.6	4.6	10.0	10.0	
θ_b	7.5	6.5	9.1	9.1	4.0	3.9	3.7	3.7	9.2	9.2	
R_{ja} (°C/W)	18.2	16.0	15.1	15.1	7.4	7.2	7.0	7.0	15.9	15.9	
Ropt (°C/W)	3.7	3.7	3.8	3.8	4.4	4.4	4.4	4.4	6.8	6.8	
Fopt (%)	20	23	25	25	59	61	63	63	43	43	
R_{ja}^{v} (°C/W) .	43	43	38	38	58	58	58	58	<u> </u>	-	

Table 2: Experimental and Numerical Predictions

fined, and thermal resistances were obtained for the packages studied. The optimization factors given in this study can be viewed as only partial estimates for a complete understanding of package optimization. The effects of heat sinks, and various cooling and geometric variations would need to be studied before reassessing the actual package design for thermal optimization. This would then constitute a package optimization strategy, a process by which the thermal design could be more clearly undertaken.

It is recommended that natural convection simulations be performed which could be compared directly to the R^v_{ja} values quoted. Also, further testing needs to be done addressing die pad resistances, and discrepancies which were obtained with regards to ceramic package case temperatures. Experimental and numerical studies are presently proceeding for multiple-chip and pin-grid array packages.

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