F_{opt} - A Thermal Optimization Factor For Microelectronic Packages

by

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ABSTRACT

In this work, thermal resistance characterization of typical microelectronic packages is presented in terms of an optimization factor, which can provide a useful standard for design and modelling package performance. The present, inconsistent use and definition of junction-to-ambient thermal resistance is addressed, by outlining the dependence of package thermal performance on the actual operating environment.

The various heat flow paths from a typical module are outlined, and a variety of package types are modelled, including single-chip and multi-chip packages. Numerical and experimental data is shown for typical microelectronic packages in use in the industry. The importance of mounting a package on a printed circuit board and its effect on the estimation of thermal resistances is discussed in detail.

Theoretical issues such as isothermal package assumptions, estimation of film coefficient, and two-sided circuit boards are addressed. The study shows that the optimization factor and associated thermal resistances provide a more concise modelling approach to thermal analysis of microelectronic packages.

Nomenclature

A_j	junction surface area, m^2
A_{PB}	package-board interface area, m^2
A_s	total package surface area exposed to ambient cooling conditions, m^2
$\mathcal{F}_{opt}$	thermal optimization factor, %
H	package height, m
h	convective film coefficient, W/mK
k_B	PCB thermal conductivity, W/mK
k_f	thermal conductivity of ambient medium, W/mK
L_B	characteristic board length, m
L_1	package length, m
Nu	dimensionless Nusselt number
Q_b	PCB heat flow at package location, W
Q_j	total junction heat flow, W
R	thermal resistance, $°C/W$
R_{ja}	junction-to-ambient thermal resistance, $°C/W$
R_{jb}	junction-to-board thermal resistance, $°C/W$
R_{jc}	juntion-to-case thermal resistance, $°C/W$
R_{ca}	case-to-ambient thermal resistance, $°C/W$
R_{ba}	board-to-ambient thermal resistance, $°C/W$
R_{max}	maximum package thermal resistance, $°C/W$
R_{nat}	package thermal resistance under natural convection cooling only, $°C/W$
R_{opt}	optimum package thermal resistance for isothermal case conditions, $°C/W$
T_B	board (PCB) temperature, $°C$
T_j	mean package junction temperature, $°C$
T_c	mean package case temperature, $°C$
T_f	local ambient mean temperature, $°C$
T_{top}	mean top of package case temperature
U_∞	ambient coolant flow velocity, m/s

Greek Symbols

θ	temperature rise above ambient, $\equiv T - T_f, °C$
∂	partial derivative

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1 Introduction

Thermal resistance characterization of microelectronic package components has often been reported in terms of a junction-to-ambient thermal resistance, R_{ja}. Unfortunately, as noted by [1,2,3,4], a specific R_{ja} value will not adequately reflect the dependence of package thermal performance in the actual operating environment. If the package is mounted on a printed circuit board (PCB), then the board temperature, hence board thermal resistance, will directly affect any package solution for R_{ja}.

The complete thermal resistance network for a single-chip package (SCP) is illustrated by the schematic in Fig. 1. R_{ca} is the case-to-ambient, and R_{ba} is the board-to-ambient thermal resistance. The resistances R_{ba}, R_{ca} cannot be neglected, since they are direct components of the heat flow analysis, and therefore must be inherent in any procedure used for estimating junction temperature rise. R_{ja} is properly defined as

$$R_{ja} = \frac{\overline{T_j} - T_f}{Q_j} = \left(\frac{1}{R_{jc} + R_{ca}} + \frac{1}{R_{jb} + R_{ba}} \right)^{-1} \qquad (1)$$

This shows that any experimental or numerical estimate of R_{ja} will be dependant on the package construction (R_{jb},R_{jc}), the package cooling conditions (R_{ca}), and the circuit board thermal resistance (R_{ba}).

The form (1) embodies all the possible heat flow paths that exist within an SCP except for microchannel and/or heat pipe cooling of packages, or where liquid cooling to another ambient heat sink is considered. This form of R_{ja} is valid for typical microelectronic packages currently in use in the industry, such as dual in-line (DIP), pin grid array (PGA), ceramic and plastic quad packages (CQUAD, PQUAD) plastic leaded chip carrier (PLCC), and leadless ceramic chip carrier (LLCCC). Also, it readily holds for single and multiple package boards.

The details pertaining to particular package construction become part of the package resistances, R_{jb}, R_{jc}. The junction-to-board thermal resistance, R_{jb}, must include all heat flow paths to the circuit board. There are essentially two such paths, as shown in Fig. 2, namely through the leadframe attachment, and from the bottom surface of the package via radiation and conduction. A mean board temperature is usually assumed at the package-to-board mounting location. The leadframe attachment could also accomodate mounting of the package to a socket assembly, which in turn is attached to the PCB. A combined package-socket assembly was neatly discussed in [1].

R_{jc} is the junction-to-case thermal resistance which models the heat flow paths between the junction and the package casing, from which heat will directly escape to the ambient T_f eventually through R_{ca}. It is important to note the distinction between R_{jc} and R_{jb} given special instances. Even if the PCB was presumed to be at ambient temperature T_f, then $R_{ba} \equiv 0$, but the form (1) still shows that R_{jc} and R_{jb} have independent flow paths. If the package was completely detached from a board mounting, then R_{jc} and R_{jb} could be combined as one R_{jc} value. This shows the error that is introduced in quantifying R_{ja} as per a vendor-supplied thermal resistance under natural or forced convection conditions, since the mere mounting of the package to a PCB completely modifies the form of the R_{ja} expression, affecting directly the estimation of chip junction temperature. Additionally, a vendor-supplied value of R_{ja} under natural convection conditions should not be considered as a standard specification, since inherently natural convection cooling implies a relatively low film coefficient, resulting in high junction temperature. Combined with the relative sensitivity of natural convection experiments, which have shown to yield very different R_{ja} values depending on the test enclosure particulars, [1], clearly a more suitable standard, if any, should be determined.

R_{ca} is the case-to-ambient thermal resistance, which includes both radiation, conduction and convective heat losses from the exposed surfaces of the package to the ambient fluid T_f. Usually a single uniform convective film coefficient is assigned to all package surfaces which are exposed to the ambient. This is generally applicable to the top and side surfaces of a package, however as can be seen from Fig. 2, the bottom package surface, when not flush-mounted to the PCB, also loses heat to the surrounding ambient. For typical microelectronic packages, the package-to-board gap is on the order of 10^{-3} m. Flow simulations have shown that the corresponding film coefficient beneath the package is much lower than that found on the other surfaces [5], since the predominant flow path is up and over a low profile package mounted on a PCB. R_{ba} is the board-to-ambient thermal resistance, which includes the conduction resistance through a particular PCB and the film resistance on the top and/or bottom exposed surfaces of the PCB.

The use of R_{ja} has become fairly standard in the industry, and rather than replacing standard supplied values, Andrews [1] proceeded with justified modification to its definition. This study aims to clarify appropriate thermal modelling techniques in order to be able to compare the thermal performance of packages under a more standard reference.

An optimal cooling configuration for a typical package could be realized if all external package surfaces were maintained at ambient temperature, resulting in an *isothermal-case* package. This effectively removes R_{ca}, R_{ba} from the calculations. We thus define

$$R_{opt} = \frac{\theta_{opt}}{Q_j} = \frac{T_j - T_c}{Q_j}; \; T_c \equiv T_f \qquad (2)$$

as being the isothermal-case package resistance, and additionally define a *percentage optimization factor*

$$\mathcal{F}_{opt} = 100 \frac{R_{opt}}{R_{ja}} \qquad (3)$$

A value of R_{opt} cannot be precisely obtained from experiment, and therefore only an accurate theoretical-numerical estimate would have to suffice. Vendor-supplied, standard values of R_{opt}, rather than R_{ja} under natural or forced conditions, would probably best serve the needs of package design and optimization, as concurred by [2]. Typical R_{ja} determination for a package in an enclosure under natural convection conditions was outlined in [6]. Unfortunately, the natural convection for a package in an enclosure differs from a package mounted on a printed circuit board. A figure-of-merit factor (FOM) was introduced [1], accounting for the configuration dependance of R_{ja}, which removed R_{ba} from the analysis, but not R_{ca}. The FOM factor is a subset of $\mathcal{F}_{opt}$ for optimization purposes.

In this work we will examine a number of important issues regarding package thermal modelling and optimization. Firstly, several packages are examined using the $\mathcal{F}_{opt}$ optimization factor introduced above. This then leads into a look at approximations concerning actual non-isothermal packages, and some effective modelling techniques. Included is a discussion concerning the effectiveness of heat sink attachment on actually reducing junction temperature. A section is devoted to an outline of current R_{ca} models which estimate the local package film coefficient, and comparisons are noted between several models. The use of R_{jb}, R_{jc} for PCB analysis is described, which forms the basis for effective determination of junction temperature rise. This type of procedure is in use with META [7], an analytically based PCB-package thermal analyzer. A discussion is also made concerning the necessary modifications to equation (1) for multi-chip packages (MCPs).

2 $\mathcal{F}_{opt}$ Modeling

The definition of the optimum package resistance R_{opt} in eq. (2) assumes that a package has case temperature T_c specified as uniform over its surfaces. Since Q_j, the applied heat power to the chip is assumed fixed, then the junction temperature T_j will need to be computed based on particular T_c values. For instance, a microelectronic package operating under two different ambient system temperatures would of course have two separate estimates of T_j based on the form (2).

Several typical microelectronic packages were analyzed in [8], and we will use these in this study to examine optimum package modelling. Two typical SCP packages one considered here, namely a 68 pin plastic quad (PLCC), and an 84 pin ceramic quad (CQUAD). Values of R_{opt} and $\mathcal{F}_{opt}$ are shown in Table 1 for the referenced packages. Also shown are R_{ja} values which were obtained under the forced convection operating conditions, with flow velocities as shown. The package film coefficients and ambient system temperature are shown, as obtained from [8]. Additionally, the mean junction temperature rise, and top of package temperature rise ($\theta_{top} \equiv T_{top} - T_f$) are noted. Vendor supplied R^{v}_{ja} values obtained under natural convection conditions are supplied also.

Table 1 shows that, under the typical system operating conditions of the packages, as they were tested experimentally, their performance assessed using the $\mathcal{F}_{opt}$ criterion is quite poor. When an optimum heat sink was attached to the top or bottom surfaces of each of these packages ($h \rightarrow \infty$ at the exposed top or bottom surfaces), with the remaining surfaces having the specified film coefficient as noted, the results that were obtained are shown in Table 1. Respectively, the packages could be considered as isothermal-cap and isothermal-base.

Although the assumption that h_{top} or $h_{bot} \rightarrow \infty$ is not quite achievable from standard heat sinks available to the industry, the results however give a clear indication of the heat flow paths within these typical package modules. For the ceramic packages, which were of a cavity-up die configuration, the top surface cap attachment of a heat sink is seen to be not anywhere near as effective as when a bottom surface attachment was made. However, the opposite results could be realized if the packages had a cavity-down die arrangement.

The results from Table 1 clearly show the tremendous possibility of reducing junction temperatures in typical microelectronic packages. Given the standard package design, hence a value of R_{opt}, a relative measure of performance can be determined under typical operating conditions. Clearly, a quick, optimum operating junction temperature could be estimated using R_{opt} for the particular package given on ambient temperature. This naturally raises the possibility of estimating the worst operating condition, or conversely an R_{max}, which could predict the maximum junction temperature for a particular package. Use of R_{nat}, a natural-convection package thermal resistance, has often times been reported for this type of measure, however inconsistencies in experimental conditions have led to a variation of reported R_{nat} values. As a result, we consider a more fundamental alternative.

The extreme condition, as all package surfaces approach insulation, is too harsh an extremum to use as R_{max}. It is therefore proposed that the diffusive limit for convection from an isolated body [9,10] be used. Any form of natural, forced or mixed convection, and radiation heat transfer will achieve a surface film coefficient larger than the diffusive limit value.

The diffusive limit may be approximated by the dimensionless form of Nusselt number [10] as

$$Nu = 3.385 + 0.082\left(\frac{L_1}{H}\right) \quad (4)$$

$$= \frac{h\sqrt{A_s}}{k_f} \quad (5)$$

where A_s is the total package exposed surface area, H is the package height, and k_f is the thermal conductivity of the ambient medium.

A more general form of (4), applicable to arbitrary isopotential bodies was proposed in [11], which describes to with $\pm$ 5%, the diffusive limit to be

$$Nu = 3.45; \pm 5\% \quad (6)$$

Any natural convection system will have a Nusselt number greater than the form (4). This then provides a convenient, lower bound estimate of the film coefficient over a package, which immediately can lead to a very accurate prediction of the maximum possible operating junction temperature.

We will therefore define an R_{max} by

$$R_{max} = \frac{\theta_{max}}{Q_j} = \frac{T_j - T_f}{Q_j} \quad (7)$$

where all the package surfaces have an h film coefficient as determined from (4) or (6).

$$h = \frac{k_f \, Nu}{\sqrt{A_s}} \quad (8)$$

Values of R_{max} are also shown in Table 1 for the packages being studied, where the form (6) was used to establish the film coefficient in (8). The fluid medium was taken as air, with $k_f = 0.026 \; W/mK$, and the respective areas

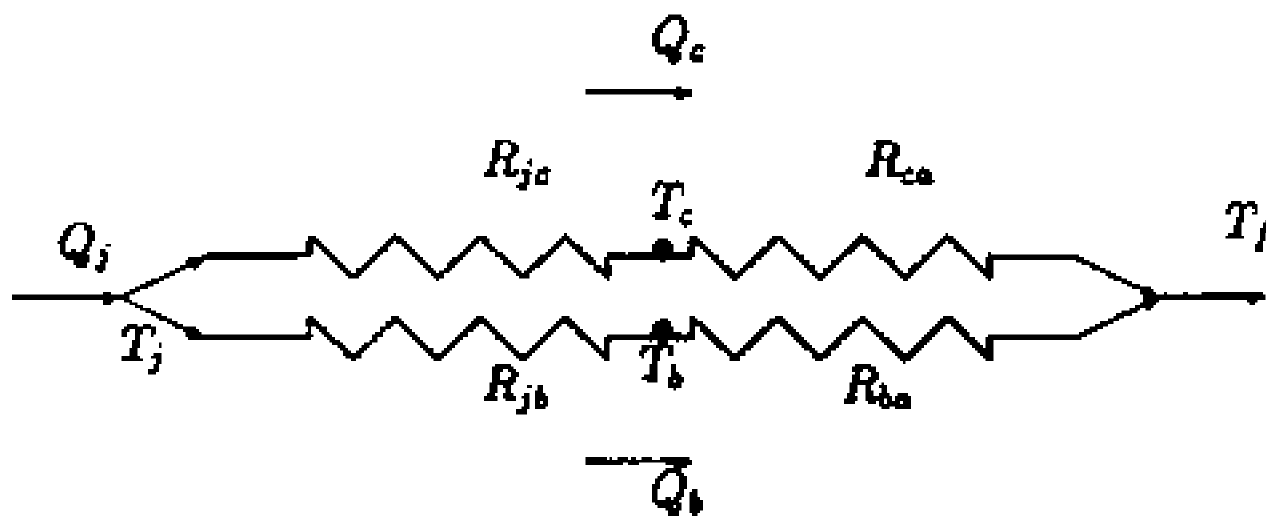

Figure 1: SCP Thermal Resistance Network

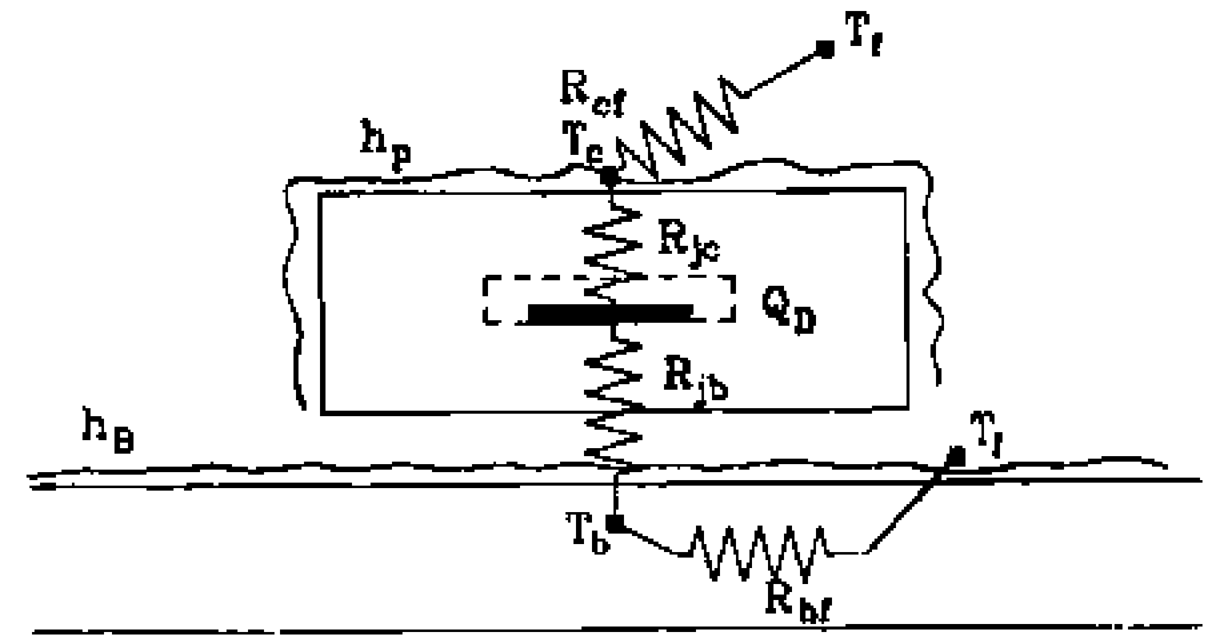

Figure 2: Resistance Modelling

	PLCC		CQUAD	
Q_j	0.5	0.5	0.5	0.5
U_∞	3.5	5.1	3.5	5.2
T_f	20.9	20.0	21.5	21.5
Experimental Temperatures				
θ_{top}	5.2	5.4	4.1	2.9
θ_j	12.2	11.3	11.8	10.9
R^v_{ja}	43	43	38	38
Numerical Predictions				
h_{avg}	45.2	53.6	48.8	58.5
θ_{top}	7.4	6.3	3.8	2.8
θ_j	9.5	8.3	13.9	13.0
R_{ja}	19.2	16.6	27.2	25.5
Optimum Package Predictions				
R_{opt}	2.7	2.7	1.1	1.1
$\mathcal{F}_{opt}$ (%)	15	17	4	4
$h_{top} \to \infty$ Predictions				
θ_j	2.6	2.5	13.1	12.5
R_{ja}	5.0	5.0	25.7	24.5
$\mathcal{F}_{opt}$ (%)	54	54	4	4
$h_{bot} \to \infty$ Predictions				
θ_j	8.8	8.0	1.0	1.0
R_{ja}	17.3	16.0	1.2	1.2
$\mathcal{F}_{opt}$ (%)	16	17	92	92
Diffusive Limit Predictions				
h	2.3	2.3	2.0	2.0
θ_j	18.4	18.4	135.5	135.5
R_{max}	36.8	36.8	267	267
$\mathcal{F}_{opt}$ (%)	7	7	0.4	0.4

Table 1: PLCC and CQUAD Package Simulations ([1])

were: PLCC, $A_s = 0.001568\ m^2$; CQUAD, $A_s = 0.001923\ m^2$. Other pertinent details may be found in [8].

The results offer some very useful insight into the thermal behaviour of plastic and ceramic -type packages currently being used in the industry. It is important to note that the PLCC contained a highly conductive leadframe ($k = 300\ W/mK$) compared to the CQUAD ($k = 11\ W/mK$). The numerical predictions agree quite closely, with $2-3°C$, of the experimental data. The h_{avg} shown was obtained using the PCB modeler [7], in conjunction with the package modeler [8]. The R_{ja} predictions of the experiment, under 2 different flow velocities shown, are about half the reported R^v_{ja} for natural convection conditions.

The heat sink attachment studies, although optimum, distinctly show the differences between the two types of packages. For the PLCC (plastic $k = 0.63\ W/mK$), having cap thickness equal to half of its substrate (beneath die) thickness, the condition $h_{top} \to \infty$ appears more favourable. For the CQUAD (ceramic $k = 16.7\ W/mK$), the reverse situation, i.e. $h_{bot} \to \infty$, provides better performance enhancement. It is important to remember that the ceramic package had a cavity-up die configuration. Interestingly, there is a tremendous $\mathcal{F}_{opt} = 92\%$ realization for the ceramic package, compared to the plastic package $\mathcal{F}_{opt} = 54\%$. This can be explained by the difference in thermal conductivities used for the packages.

The diffusive limit predictions show that the ceramic package performance is strongly affected by the film coefficient specified. Indeed, R_{max} is well above the R^v_{ja} value. Further numerical validation is needed to verify this finding. For the PLCC, it appears that R^v_{ja} is unaccountably larger than R_{max}; further details concerning reported experimental values need to be looked into.

3 R_{jb}, R_{jc} For PCB Analysis

The separate package thermal resistances R_{jb}, R_{jc} can be incorporated quite adequately within a PCB modeller framework, which is used to compute specific local film coefficients and board temperatures. A PCB modeller, such as META, [7], uses specified local package heat fluxes, which are input to the flow field and board. The flow (coolant) local ambient temperatures and film coefficients are strong, positionally dependent functions of heat fluxes which are leaving the board/package surfaces. However, the magnitude of these heat fluxes are directly influenced by the ratio of R_{jb} to R_{jc}.

The procedure for including R_{jb}, R_{jc} into a generic PCB analyzer, which determines T_B and R_{ba} will now be briefly outlined. It is assumed that the fluid-solid interface boundary condition is of a general convective form. At package (heat source) locations, this boundary condition can be modified to the form

$$L_B \frac{\partial T_B}{\partial n} + Bi\, f_{jb}\,(T_B - T_f) = \frac{Q_j\, L_B\, f_{jb}}{A_j k_B} \qquad (9)$$

where f_{jb} is defined as

$$f_{jb} = (1 + h/h_{jb})^{-1} \qquad (10)$$

and we have defined

$$Bi = \frac{hL_B}{k_B} \qquad (11)$$

$$h_{jb} = (A_{PB} R_{jb})^{-1} \qquad (12)$$

The film convection coefficient h is a modified coefficient combining an effective conductance from R_{jc} and the fluid side film coefficient h_f in R_{ca}.

Thus,

$$\frac{1}{hA_s} = R_{jc} + R_{ca} \qquad (13)$$

where A_s now signifies only the package surface (i.e., case) that is exposed to the flow.

The discrete form of (9), applied to the PCB system with arbitrarily located packages, determines the local board temperatures T_B, from which R_{ba} is readily determined,

$$R_{ba} = \frac{\overline{T}_b - T_f}{Q_b} \qquad (14)$$

where $\overline{T}_b$ is the mean board temperature at a particular package location, and Q_b is the total heat flow entering the board from the supplied package power (i.e., $Q_b \geq Q_j$).

4 MCP Thermal Analysis

The analyses up to this point have centered on SCP systems where there is a single heat source die, residing within the package. Multi-die systems are also fairly common to the industry, and to characterize these multi-chip packages (MCPs) some minor adjustments are necessary to the earlier definitions.

A double-chip thermal resistance analog is shown in Fig. 3. By having more than one die (chip) in the package, the individual $R_{jb} - R_{jc}$ network are in parallel format given that common package case and board attachments are assumed. Since supplied heat flux levels to particular chips may differ, it is possible to define two distinct resistances. The form (2) applies to each individual chip of the MCP, and also, an overall MCP resistance would be:

$$R_{opt} = \frac{\overline{T}_j - T_c}{\sum Q_j};\ (MCP)$$

The individual chip thermal resistance is basically the same as eq. (2). The overall package resistance involves a mean-junctions temperature $\overline{T}_j$, as well as an overall heat supply $\sum Q_j$. Since many MCP systems involve more than two chips residing within the package, it would appear that both the forms (2) and (8) would provide useful information to the package analyst. However, individual chip resistances could be much larger than the overall MCP resistance, and individual chips could have higher junction temperature levels.

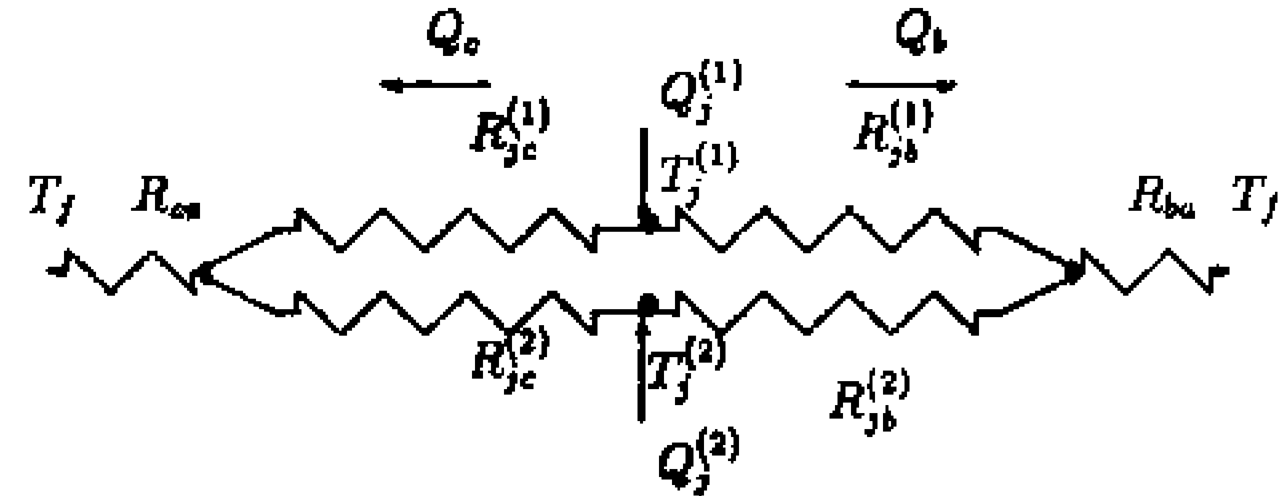

Figure 3: MCP Thermal Resistance Network

5 Summary and Conclusions

The aim of this study was to provide a more coherent standard for microelectronic package performance assessment. An optimum package thermal resistance and optimization factor were defined, which can be used by a thermal designer to measure the variation of performance under given system constraints. These system constraints and the individual thermal resistances existing for any package-on-board arrangement were outlined, and shown to hold for both SCP and MCP designs.

A convenient upper bound on the thermal resistances of packages was introduced, based on the diffusive limit of heat flow from arbitrary body shapes. R_{ja} values obtained from natural convection experiments, which may differ, must lie within the bounds determined by this study.

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